REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 12 July 2004. Responsive to the rejections made by the Examiner in the Official Action, Claims 1, 3, 6, 7, 9, 11-14, and 16-18 have been amended and Claims 2, 4, 8, 10 and 15 have been canceled. The presently pending Claims 1, 3, 5-7, 9, 11-14, and 16-18 are now more clear in their respective recitations.

In the Official Action, the Examiner rejected Claims 1 and 3-5 under 35 U.S.C. § 102(e) as being anticipated by Watts, Jr., et al. (U.S. Patent Application Publication U.S. 2002/0103005; hereinafter Watts). The Examiner stated that Watts discloses a circuit system for data transmission between LPC devices coupled to first and second LPC busses and referred particularly to Fig. 3 and paragraph [0026] in making the rejections.

The Examiner rejected Claims 6-10 and 13-19 under 35 U.S.C. § 102(e) as being anticipated by Shaw (U.S. Patent 6,732,216). The Examiner stated that Shaw discloses a method for data transmission between LPC devices on separate LPC busses and when coupled to the same LPC bus. The Examiner also stated that, with regard to the insertion of wait states in the first LPC bus cycle, the "set of registers (transactions) implies transactions in wait states".

In the Official Action, the Examiner rejected Claims 2 and 11-12 under 35 U.S.C. § 103(a) as being unpatentable over Watts in view of Shaw. The Examiner stated that Watts discloses all of the claimed limitations except where the LPC

host controller or the master LPC device further includes an address register. The Examiner then cited Shaw as disclosing typical computer architectures that provide for a set of registers, where each register is assigned to a particular peripheral or I/O device. The Examiner then stated that the information contained in the registers provide addresses and access content to the CPUs and concluded that it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Shaw into the system of Watts "so as to provide maximum processing capability for the multiple systems in the computer architecture, allow continuous processing and computing and avoid the need to reset or place in a suspend state any or all of the processors".

Prior to addressing the cited reference with respect to Applicant's system and method for data transmission between LPC devices, it is believed beneficial to first briefly describe the structures of the invention of the subject Patent Application and procedures executed thereon in light of the currently amended Claims, the Specification and the Drawings. The present invention generally provides means by which data may be transmitted between low pin count (LPC) devices, in accordance with the LPC interface specification to increase data throughput in an LPC implemented system.

As is well known in the art, the LPC interface allows support for legacy I/O configurations to support an industry-wide transition from ISA bus-based systems to PCI bus-based systems. To that end, Intel Corporation drafted the well known

LPC interface specification to provide a standardized implementation to facilitate a stable migration from the ISA/X-bus to the LPC interface, while retaining full software compatibility.

One of the limitations of the LPC interface is identified in Fig. 1 and Figs. 2a-2b of the subject Patent Application. As is shown in the Figures, every bus transaction is initiated by the host controller and is terminated with the host controller having solitary access and control over the LPC bus. Thus, there is no mechanism for accessing data on an LPC device coupled to the LPC bus by another LPC device simultaneously coupled to the same LPC bus within a single bus access cycle. The LPC devices do not have means to maintain the address of data on any other LPC device over multiple bus access cycles and, thus, data transfer requires external temporary data storage. Among other things, the present invention overcomes this shortcoming of the prior art, while still maintaining adherence to the LPC interface specification.

According to a first embodiment of the present invention, an address register for storing a target address of a data transfer transaction is installed in the LPC host controller. This allows the necessary linkage in forming a data transmission path from one LPC device to another. The LPC host controller is then operable to initiate a first bus access cycle on a first LPC bus. A second bus access cycle on a second LPC bus is commenced when the LPC host controller determines that a target address stored in the address register is that on a second

LPC device coupled to the second LPC bus. The first LPC bus cycle is terminated only after the second bus access cycle is terminated.

In certain embodiments of the invention, operations on the first LPC bus are suspended by the insertion of wait states in the first bus access cycle. Applicant makes note that the term "wait state" is used in the subject Patent Application in accordance with its usual definition in the computing art. As is widely known, such wait states are implemented to intentionally suspend computer operations over some time interval.

In other embodiments of the invention of the subject Patent Application, the LPC host controller, a master LPC device and one or more slave LPC devices are coupled to an LPC bus. Each of the LPC devices and the LPC host controller are provided with an address register to store an address of a target data location. The LPC host controller is operable to initiate a data transfer cycle including a first bus access cycle, during which the master LPC device has access to the LPC bus, and a second bus access cycle, during which a slave LPC device has access to the LPC bus.

In certain embodiments of the invention, a request for a transaction is transmitted from the master LPC device to the LPC host controller so as to specify a transfer of first data between the master LPC device and a slave LPC device. During the first bus access cycle, second data is transferred between the LPC host controller and the master LPC device. In some embodiments, if the transaction is

a data read operation from the slave LPC device, the second data is set to an arbitrary data value. In other embodiments of the invention, if the transaction is a data write to the slave LPC device, the second data is set equal to the first data.

Once the second data has been transferred between the LPC host controller and the master LPC device during the first bus access cycle, the address of the data location on the slave LPC device is stored in the address register of the master LPC device. The second bus access cycle is then initiated on the LPC bus, during which the first data is transferred between the slave LPC device and LPC host controller. In some embodiments of the invention, during a data read operation, the LPC bus is monitored for data transferred from the slave LPC device and is accepted by the master LPC device as the first data if the source address of the data matches the address stored in the master LPC device's address register.

In contradistinction with the present invention, the prior art references cited by the Examiner do not address the problems encountered when a first LPC bus device wishes to access a data location on a second LPC device. Watts is directed to synchronizing data on a personal digital assistant (PDA) with a personal computer (PC) and vice-versa. Both the PDA and PC are adapted to receive messages from a communication device and the data in one device are synchronized with that in the other by the disclosed process. However, Watts does not demonstrate direct access to one device by another by including "an LPC host controller including an address register for storing a target address, said LPC host

controller being operable to initiate a first bus access cycle on [a] first LPC bus and a second bus access cycle on [a] second LPC bus", as now recited by the amended Claims of the subject Patent Application. As further recited in the amended Claims, the LPC host controller is configured to "initiate said second access cycle upon said target address matching an address on said second LPC bus" and to "terminate said first bus access cycle only after said second bus access cycle is terminated". As opposed to the direct access of the present invention, as now claimed, Watts instead demonstrates synchronization using a common storage facility, such as the hard drive of the PC, access to which is available to both devices. In fact, synchronization of data between devices does not necessitate direct access to a storage location on one device by addressing that location on another device. Thus, whereas Watts has some structural elements in common with that of the invention of the subject Patent Application, the disclosure is directed to another purpose and therefore does not disclose, or even suggest the advantageous combination of features provided for by the invention of the subject Patent Application.

The disclosure of Shaw is directed to allowing a computer system to continue full processing and computing operations while another system is in control over commonly shared peripherals and I/O devices. Shaw does not illustrate how the PC has access to memory of the PDA, or vice-versa, and, in fact, states that when the PDA has access to its set of registers, it treats the PC as being

non-existent. Further, the registers disclosed by Shaw are not adapted in any way to facilitate the transfer of data from either the PC or PDA to the other device by the steps of "providing an LPC host controller with an address register for storing a target address", "storing an address of a data location on said second LPC device in said address register" and "accessing by said LPC host controller said data location over said second LPC bus", as is now clearly recited by the newly amended Claims. Instead, the registers of Shaw are used in communication by one of the PDA or PC (the slave device and master device, respectively) to an associated peripheral device. Thus, the registers of Shaw are used to contain operational data of the associated peripheral device and are not used to store an address to access a memory location so as to facilitate master/slave data transferal. As such, the registers do not equate to being "address registers" but, instead, are "data registers".

Shaw does not disclose the step of "inserting a plurality of wait states in said first bus access cycle", as now recited by the amended Claims. Contrary to the Examiner's assertion that a "set of registers (transactions) implies transactions in wait states", data held in a register pending a computing operation does not imply the insertion of wait states per the conventional definitions of the art. Nor does Shaw anywhere disclose or even suggest that any computer operations are suspended while data are held in the registers. Moreover, there is no common understanding in the art that data held in a register pending a computer operation

implies the insertion of wait states, and Shaw makes no suggestion of such understanding. It would be nothing less than improper hindsight reconstruction to nonetheless insist that the mere disclosure by Shaw of registers necessarily implies certain wait states.

Neither Watts nor Shaw nor the combination thereof disclose or suggest a circuit system for data transmission between LPC devices comprising a "master LPC device including an address register for storing a target address" and an LPC host controller including "an address register for storing said target address", so as to "initiate a data transfer cycle on said LPC bus, said data transfer cycle including both a first bus access cycle for LPC bus access by said master LPC device and by a second bus access cycle for LPC bus access by one of said at least one slave LPC device" as is now recited in the amended Claims of the subject Patent Application. The references individually and in combination fail to disclose a system or a method by which data is transferred from one LPC device to another over one or more LPC busses as does the invention of the subject Patent Application, as now claimed.

Thus, as the references fail to show each and every element of the invention of the subject Patent Application, as now recited in newly amended independent Claims 1, 6, 11 and 13, it is believed that neither reference can anticipate the invention so claimed. Additionally, as the combination of references cited by the Examiner fails to disclose the unique combination of elements for the purposes of

LPC inter-device communication, the references cannot make obvious that invention, either. Thus, independent Claims 1, 6, 11 and 13 are now believed to be in condition for allowance. That being so, pending Claims 3 and 5, which are ultimately dependent from independent Claim 1, pending Claims 7 and 9, which are ultimately dependent from independent Claim 6, pending Claim 12, which is dependent from independent Claim 11, and pending Claims 14 and 16-18, which are ultimately dependent from independent Claim 13, are believed to be allowable for at least the same reasons for which their respective base Claims are allowable.

The remaining references cited by the Examiner, but not used in the rejections, have been reviewed, but are believed to be further remote from the subject Patent Application than the references used by the Examiner when patentable considerations are taken into account.

It is now believed that the subject Patent Application has been placed in condition for allowance and such action is respectfully requested.

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